



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,300	11/08/2001	Keiji Jono	KM1-003	4689
21567	7590	03/16/2004	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			TRAN, THIEN F	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/007,300

Applicant(s)

JONO ET AL.

Examiner

Thien F Tran

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 42-47 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 42-47 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/21/2004 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 42-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (USPN 6,034,409) in view of Wu (USPN 6,355,540).

Sakai et al. discloses a trench isolation structure (Fig. 7) formed in a semiconductor 1 comprising a first isolation trench portion 11a having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle A1; a second isolation trench portion 11 within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle A2 with respect to the surface that is greater than the first angle, the second isolation trench portion having a

Art Unit: 2811

bottom portion at the second depth of the semiconductor; and a dielectric material 4 filling the first and second isolation trench portions. Sakai et al. does not disclose the semiconductor at the bottom portion of the trench structure being doped. It is old and well known in the art to form a channel stop region (doped region) beneath the trench structure in the semiconductor substrate as shown for example by Jun. Jun discloses forming channel stop regions (doped regions 20) beneath the trench (see Fig. 2F). Therefore, forming the trench isolation structure of Sakai et al. comprising a channel stop region (doped region) beneath the trench structure would have been obvious modification in order to restrain stress caused by oxidation of the semiconductor substrate and to improve the insulation properties of the trench isolation structure.

Regarding claim 43, at least some of the first isolation trench portion forms a substantially straight linear segment.

Regarding claims 44 and 45, the first angle A1 and the second angle A2 are within the claimed range.

Regarding claim 46, the first depth is between five and fifty percent of a total trench depth.

Regarding claim 47, Sakai et al. does not explicitly disclose the trench isolation structure being formed in a memory integrated circuit. However, a memory integrated circuit is a conventional structure comprising isolation structures and active devices (transistors). It would have been obvious to form the trench isolation structure of the above combined references into the memory integrated circuit for the advantages that

Art Unit: 2811

the trench structure provides as described above, to better isolate active devices from one another in the memory integrated circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are being cited since they show trench isolation structure including channel stop regions beneath the trench structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
February 24, 2004


**THIENTRAN
PRIMARY EXAMINER**